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Express Mail Label No. EL 438 938 155 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Seiichi MORI
Serial No: Not assigned
Filed: December 8, 1999
For: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith for filing is the patent application identified above.

- ☒ 3 sheet(s) of drawings (☐ formal ☒ informal) is(are) enclosed.
- ☒ 16 page(s) of specification and 1 page(s) of abstract of the invention are enclosed.
- ☒ An assignment of the invention to KABUSHIKI KAISHA TOSHIBA ☒ is enclosed ☐ will follow.
- ☐ An associate power of attorney ☐ is enclosed ☐ will follow.
- ☐ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 & 1.27 is enclosed.
- ☒ Declaration and Power of Attorney ☒ is enclosed ☐ will follow.
- ☒ A certified copy of Japanese Patent Application No. 10-350232 filed December 9, 1998 from which priority is claimed under 35 U.S.C. § 119 is enclosed.
- ☐ IDS enclosed (☐ with references).
- ☐ Preliminary Amendment is enclosed.

CALCULATION OF FEES

	ITEM	TOTAL NO. OF CLAIMS		NO. OF CLAIMS OVER BASE	LG/SM $ ENTITY FEE		$ AMOUNT	$ FEE
A	TOTAL CLAIMS FEE	18	-20	0	LG=$18 SM=$9	$18	0	
B	INDEPENDENT CLAIMS FEE*	5	-3	2	LG=$78 SM=$39	$78	156	
C	SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)							$ 156
D	MULTIPLE-DEPENDENT CLAIMS FEE						LARGE ENTITY FEE = $260 SMALL ENTITY FEE = $130	$ 0
E	BASIC FEE						LARGE ENTITY FEE = $760 SMALL ENTITY FEE = $380	$ 760
F	TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)							$ 916
G	ASSIGNMENT RECORDING FEE						$ 40	$ 40
	*LIST INDEPENDENT CLAIMS 1, 5, 7, 9 and 14							

"Continued on Second Page"

- ☒ A check in the amount of $ 916 to cover the filing fee is enclosed.
- ☒ A check in the amount of $ 40 to cover Assignment Recordation fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge any deficiency for the following fees associated with this communication or credit any overpayment to Deposit Account No. 12-1820. **A copy of this sheet is enclosed.**
  - ☒ Any additional filing fees required under 37 C.F.R. § 1.16
  - ☒ Any patent application processing fees under 37 C.F.R. § 1.17

  Please associate this application with the attorneys of record and with the correspondence address recorded for Customer No. 22335.

Respectfully submitted,
LOEB & LOEB LLP

Date: December 8, 1999

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PATENT
Attorney Docket No: 005702-20053

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Art Unit: Not assigned
Seiichi MORI	Examiner: Not assigned
Serial No: Not assigned	
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Dear Sir:

I hereby certify that

☒ two copies of a letter of transmittal

☒ check in amount of $ 916 as filing fee

☒ patent application (16 page(s) of specification; 18 claim(s); 1 page(s) of abstract

☒ 3 sheet(s) of informal drawings

☒ executed Declaration and Power of Attorney

☒ assignment of the invention to KABUSHIKI KAISHA TOSHIBA

☒ certified copy of Japanese patent application No. 10-350232 which was filed December 9, 1998 from which priority is claimed in the subject case pursuant to 35 U.S.C. § 119

☒ return postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service with sufficient postage under 37 C.F.R. § 1.10 on the date indicated above and are addressed to:

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Name of person mailing papers

Signature

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12/08/1999 gc

NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a non-volatile semiconductor memory device including a memory cell having a stacked gate structure.

Description of the Background Art

What has hitherto been known as a non-volatile semiconductor memory device uses a memory cell structure on which a floating gate is provided through a tunnel insulating layer on a semiconductor substrate, and a control gate is stacked thereon through an inter-layer insulating layer. The inter-layer insulating layer of this memory cell normally involves the use of a so-called ONO (Oxide-Nitride-Oxide) structure composed of a silicon oxide layer, a silicon nitride layer and a silicon oxide layer.

FIGS. 4A and 4B show sections, taken in two directions orthogonal to each other, of the memory cell structure described above. Normally in a flash memory, the control gate of the a plurality of memory cells are consecutively arranged and serve as word lines. FIG. 4A is the section in the direction parallel to a direction of the word line.

An element isolation insulating layer 2 is provided on a p-type silicon substrate 1, and a floating gate 4 is provided through a tunnel insulating layer 3 on a device region defined by the element isolation insulating layer 2. Provided on the floating gate 4 is an ONO layer 5 as an inter-layer insulating layer including a silicon oxide layer 5a, a silicon nitride layer 5b and a silicon oxide layer 5c which are stacked in this sequence. Further, a control gate 6 is provided on the ONO layer 5. Source/drain diffused layers 7, 8 are provided in self-alignment with the control gate 6.

The ONO layer 5 functions to prevent electric charges

accumulated in the floating gate 3 from leaking out during a writing process to the memory cell, and, because of a necessity for confining the electric charges within the floating gate 4 over a long period of time, is required to exhibit a high insulating property. In the normal flash memory, the floating gate retains electrons. In an electron accumulating state, however, a comparatively weak electric field (a self electric field) generated by the electrons is applied to the ONO layer 5.

Te silicon oxide layer 5a, on the side of the floating gate 4, of the ONO layer 5, if a layer thickness thereof is 5 - 6nm, works as a Fowler-Nordheim type tunnel current conductive mechanism, wherein the electric current flowing with a low electric field is extremely small. Further, a barrier height of the silicon oxide layer 5a with respect to silicon is as high as 3.2 eV. Accordingly, if the silicon oxide layer 5 has no defect and there is no electric field enhancement effect based on a two-dimensional configuration of the floating gate 4, only the silicon oxide layer 5a must be capable of sufficiently retaining the electrons for a long time. In fact, however, there exist the defect and the two-dimensional electric field enhancement effect, and hence the ONO layer is used.

The two-dimensional electric field enhancement effect is typified by, for example, as indicated by a broken line A in FIG. 4A, an electric field enhancement at an edge which is obtained by forming the floating gate 4 in pattern. Further, there is an electric field enhancement caused by a rugged area formed on the surface of the floating gate 4 when the silicon oxide layer 5a is formed by thermal oxidation. The silicon nitride layer 5b of the ONO layer 5 contains much of trap level, and trapping occurs even when the electric current flows due to the electric field enhancement and acts to relieve the electric field, thereby restraining a leak of the electric charges from the oxide layer 5a surrounding the floating gate. If

the oxide layer 5a has a defect, the same mechanism works. This is the reason why the silicon nitride layer 5b is used.

Incidentally, when the memory cell operates, and when in a state of the electrons being held by the floating gate, a positive bias is applied to the control gate 6. It is known that a large leak current flows to the silicon nitride layer through the trap level by a hole conduction. Accordingly, supposing that the control gate 6 is provided directly on the silicon nitride layer 5b, the holes from the control gate 6 are injected, and therefore an dielectric strength is unable to be kept well. The silicon oxide layer 5c is provided upward in order to restrain the holes from being injected from the control gate 6.

The upper and lower silicon oxide layers 5a, 5c of the ONO layer 5 are each required to have a thickness of 5 - 6nm for exhibiting functions of relieving the electric field and preventing the leak. The silicon nitride layer 5b has a thickness on the order of 10nm (converted into 5nm in the case of the oxide layer). Hence, an equivalent oxide thickness of the ONO layer 5 is 15 - 16nm thick.

There arise the following problems inherent in the inter-layer insulating layer based on the ONO structure described above.

First, it is desirable for enabling the memory cell to operate at a low voltage that a capacitance coupling between the control gate and the floating gate be large. It is desirable for attaining this that the ONO layer be as thin as possible. If the layer thickness is thinned down to a limit thereof, it can be thinned totally down to approximately 14nm as an equivalent oxide thickness. However, further thinning of the layer becomes difficult.

Second, in the ONO layer, in a post-oxidating step after gate definition processing, as shown in FIG. 4B, a bird's beak B intrudes in a portion between the floating gate 4 and the control gate 6 from a side surface. The

bird's beak decreases the capacitance coupling between the control gate 6 and the floating gate 4. Especially when the silicon oxide layer 5a disposed directly on the floating gate is provided by a CVD (Chemical Vapor Deposition) method, a characteristic of density thereof is inferior to a thermal oxide layer, and hence oxygen diffuses fast within the layer, with the result that a large bird's beak occurs. In the case of obtaining the silicon oxide layer at a low process temperature, the silicon oxide layer formed by the CVD method might be used more often than by the thermal oxidation, and therefore, in such a case, the intrusion of the bird's beak turns out a problem.

SUMMARY OF THE INVENTION

It is therefore a primary object of the present invention to provide a non-volatile semiconductor memory device including an inter-layer insulating layer, which is capable of ensuring even a large capacitance coupling between a control gate and a floating gate while securing an electric field relieving effect and a leak preventive function.

According to the present invention, a silicon nitride layer having a trap level density well lower than that of a silicon nitride layer formed by a normal CVD (Chemical Vapor Deposition), especially LPCVD (Low Pressure Chemical Vapor Deposition) method, is provided in the inter-layer insulating layer, whereby a large capacitance coupling between a control gate and a floating gate can be ensured by making an effective thickness of an oxide layer smaller than in the prior art while exhibiting an electric field relieving effect and a lead reducing effect. Furthermore, if such a silicon nitride layer is disposed contiguously to the control gate or the floating gate, an intrusion of a bird's beak can be restrained from occurring in a post-oxidation step, and it is therefore feasible to ensure the large capacitance coupling between the control gate and the

floating gate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B are sectional views each showing a memory cell structure in a first embodiment of the present invention;

FIG. 2 is a sectional view showing a memory cell structure in a second embodiment of the present invention;

FIGS. 3A - 3D are sectional views showing a structure of an inter-layer insulating layer of the memory cell in a third embodiment of the present invention; and

FIGS. 4A and 4B are sectional views each showing a memory cell structure of a non-volatile memory in the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will hereinafter be described with reference to the accompanying drawings.

First Embodiment

FIGS. 1A and 1B are sectional views taken in direction orthogonal to each other, showing a memory cell structure of a non-volatile semiconductor memory device in a first embodiment of the present invention. An element isolation insulating layer 12 is provided on a p-type silicon substrate 11, and a floating gate 14 composed of a polycrystalline silicon layer is provided through a tunnel insulating layer 13 on a device area defined by the element isolation insulating layer 12. The tunnel insulating layer 13 is classified as a silicon oxide layer. A control gate 16 composed of a polycrystalline silicon layer is stacked on the floating gate 14 via an inter-layer insulating layer 15. Source/drain diffused layers 17, 18 are so provided on the substrate as to be self-aligned with the control gate 16.

The inter-layer insulating layer 15 includes a silicon

oxide layer 15a contiguous to the floating gate 14, and double-layered silicon nitride layers 15b, 15c provided thereon. The first silicon nitride layer 15b is provided by a normal CVD method, especially low pressure (LP) CVD method, and the second silicon nitride layer 15c is provided by a JVD (Jet Vapor Deposition) method. The second silicon nitride layer 15c is well lower in trap level density than the first silicon nitride layer 15b and has a less leak current at a low electric field region.

Specifically, the silicon oxide layer 15a is a thermal oxide layer obtained by thermally oxidating the floating gate 14, or a silicon oxide layer based on the LPCVD method. The first silicon nitride layer 15b is formed by the LPCVD method, wherein dichlorosilane (SiH_2C_{12}) and ammonia (NH_4) are used as raw gases. The second silicon nitride layer 15c is formed such that active Si and N are generated by plasma-decomposing a silane-series gas (e.g., SiH_4) supplied together with a carrier gas such as He etc. and a gas (e.g., N_2) containing nitrogen by microwave electric power, and supplied and deposited by the JVD method on the surface of the substrate disposed within a chamber. It has already been reported that the silicon nitride layer exhibiting a low trap level density is obtained by the JVD method (refer to, e.g., Applied Surfaces Science 177/118 (1997) 259-267). Herein, a quantity of hydrogen content of the first silicon nitride layer 15b deposited by the LPCVD method is $10^{21}/cm^3$ or more, while a quantity of hydrogen content of the second silicon nitride layer 15c deposited by the JVD method is $10^{19}/cm^3$ or less. This difference in quantity of hydrogen content therebetween correlates to magnitudes of the trap level densities of those two layers, and, in other words, the silicon nitride layer having a less quantity of hydrogen content, which is deposited by the JVD method, exhibits a low trap level density and has a smaller leak current at the low electric field region.

Note that the silicon nitride layers deposited by

other deposition methods may also be used on condition that those layers have a quantity of hydrogen content which is as small as the silicon nitride layer deposited by the JVD method, and exhibit a low trap level density.

Next, the reason why a structure of the inter-layer insulating layer 15 described above will be specifically elucidated as well as explaining a preferable thickness of each layer.

In the single layer 15c of the silicon nitride layer deposited by the JVD method, Frenkel-Poole type current, though not so much as the silicon nitride layer deposited by the LPCVD method, flows across the low electric field region, and hence this layer 15 is hard to be used solely as an inter-layer insulating layer. Further, the silicon nitride layer has a lower barrier height with respect to silicon than the silicon oxide layer, and is therefore insufficient as a barrier against a release of the electrons from the floating gate. Accordingly, it is required for forming the inter-layer insulating layer that the silicon oxide layer 15a be disposed just on, e.g., the floating gate 14. The silicon oxide layer 15a requires a thickness on the order of 5 - 6nm for keeping a sufficient dielectric strength.

This first silicon nitride layer 15b provided based on the LPCVD method is needed for preventing the lead as well as for obtaining the electric field relieving effect. That is, the first silicon nitride layer 15b exhibits a high trap density and a Frenkel-Poole type electric conductive characteristic. In this Frenkel-Poole type electric conduction, the current in a high electric field region is small, and the current becomes hard to flow through a layer containing a trap because of the carriers being trapped even when the current flows therethrough at an initial stage. Therefore, the first silicon nitride layer 15b restrains an increase in the leak current due to the electric field enhancement at the edge taking a two-dimensional configuration of the floating gate 14. It is

preferable for exhibiting the sufficient electric field relieving effect that the thickness of the silicon nitride layer 15b be over 6nm. It is also preferable for ensuring a large capacitance coupling that the above thickness be under 10nm, to be specific, on the order of 8nm.

The second silicon nitride layer 15c based on the JVD method functions to restrain the hole implantation from the control gate 16. Namely, the first silicon nitride layer 15b based on the LPCVD method is easy to flow the Frenkel-Poole type Hall current. If the silicon nitride layer 15b is contiguous directly to the control gate 6, as described above, the large leak current flows due to the hole implantation from the control gate 16 in such an operation mode that the control gate 16 comes to have a positive bias. The second silicon nitride layer 15c based on the JVD method has an extremely low trap density and effectively restrains the hole implantation from the control gate 16. It is preferable for exhibiting this function that the second silicon nitride layer 15c be over 6nm thick. It is also preferable for ensuring a large capacitance coupling that the thickness thereof be under 10nm. Specifically, for example, the thickness of the silicon oxide layer 15a is set to 6nm, and the thicknesses pf the silicon nitride layers 15a, 15b are each set to 6nm (3nm in the conversion of the oxide layer), and the effective thickness of the oxide layer is 12nm. Accordingly, the layer can be made thinner than in a case of using the conventional ONO structure, and besides the sufficient electric field relieving effect can be obtained. Further, the silicon nitride layer 15c is the uppermost layer of the inter-layer insulating layer 15, and therefore it is feasible to restrain the intrusion of the bird's beak when effecting the post-oxidation.

Second Embodiment

FIG. 2 shows, corresponding to FIG. 1B, a memory cell structure in a second embodiment of the present invention.

In the second embodiment of the present invention, the inter-layer insulating layer 15 is double-layered including two layers, i.e., from the side of the floating gate 14, the silicon oxide layer 15a and the silicon nitride layer 15c based on the JVD method which has a low trap density and a hydrogen content quantity on the order of $10^{19}/cm^3$ or less.

In the first embodiment, the silicon nitride layer 15b based on the LPCVD method and exhibiting the Frenkel-Poole type conduction, is disposed in the middle of the interlayer-insulating layer 15. If not operated with a high electric field, however, the silicon nitride layer 15b is not necessarily used. Namely, as shown in FIG. 2, for the purpose of blocking a defect in the lowermost silicon oxide layer 15a, the insulating layer may take a double-layered structure consisting of the silicon oxide layer 15a ad the silicon nitride layer 15c based on the JVD method and exhibiting the low trap density.

In the case of the silicon nitride layer formed by the normal LPCVD method and containing much of trap, the effect produced by use of the silicon nitride layer can not be expected due to a large quantity of holes injected from the control gate only with the double-layered structure of the silicon oxide layer and the silicon nitride layer. When using the silicon nitride layer based on, e.g., the JVD method, there is almost no hole conduction, and hence the above effect can be sufficiently obtained even with the double-layered structure.

Third embodiment

For preventing the bird's beak from intruding into the inter-layer insulting layer due to the post-oxidation, the silicon nitride layer formed by the JVD method and having a hydrogen content quantity on the order of $10^{19}/cm^3$ or less, is provided keeping its thickness as thin as approximately 3nm directly on the floating gate (i.e., the lowermost layer of the inter-layer insulating layer) or just under the control gate (viz., the uppermost layer of

the inter-layer insulating layer). If a layer based on the normal LPCVD method and exhibiting a high trap density is used as this silicon nitride layer, a threshold value of the memory cell might become unstable due to the trap and release of the electric charges within the layer. If the silicon nitride layer deposed by the JVD method and having a low trap density is used, however, the instability of the threshold value never occurs.

FIGS. 3A - 3D show an extraction of only the structure of the inter-layer insulating layer in the third embodiment.

FIG. 3A shows an example in which a silicon nitride layer 15d based on the JVD method is added as a layer contiguous to the floating gate 14 to a structure of the inter-layer insulating layer 15 in FIG. 15. A similar silicon nitride layer 15c serving as a layer contiguous to the control gate 16 is also provided, and the silicon oxide layer 15a is interposed between the nitride layers 15c and 15d, thereby structuring the inter-layer insulating layer 15.

FIG. 3B shows an example in which the silicon nitride layer 15d formed by the JVD method is likewise added as a layer contiguous to the floating gate 14 to the structure of the inter-layer insulating layer 15 in FIG. 1. In this case also, the similar silicon nitride layer 15c serving as a layer contiguous to the control gate 16 is also provided, and a stacked layer of the silicon oxide layer 15a and the silicon nitride layer 15b formed by the LPCVD method, is interposed between the nitride layers 15c and 15d.

FIG. 3C shows an example in which the silicon nitride layer 15d formed by the JVD method is likewise added as a layer contiguous to the floating gate 14 to a normal- ONO-structured inter-layer insulating layer 150. More specifically, the stacked layer 150 consisting of the silicon oxide layer, the silicon nitride layer based on the LPCVD method and the silicon oxide layer, is superposed

further on the silicon nitride layer 15d.

FIG. 3D shows an example in which silicon nitride layers 15d, 15e formed by the JVD method are stacked as layers contiguous to the floating gate 14 and the control gate 16, on the normal NON-structured inter-layer insulating layer 150. That is, the silicon nitride layer 15e is superposed further on the NON structured inter-layer insulating layer 150.

The third embodiment also exhibits the same effects.

According to the present invention, the silicon nitride layer having the trap level that is well lower than that of the silicon nitride layer based on the normal LPCVD method, is provided in the inter-layer insulating layer of the non-volatile memory cell having the stacked gate structure, whereby the large capacitance coupling between the control gate and the floating gate can be ensured by making the effective thickness of the oxide layer smaller than in the priori art while exhibiting the electric field relieving effect and the effect of reducing the leak.

WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate;

a first silicon nitride layer provided by a CVD method on said silicon oxide layer; and

a second silicon nitride layer provided on said first silicon nitride layer and having a lower trap density than that of said first silicon nitride layer.

2. A non-volatile semiconductor memory device according to claim 1, wherein said second silicon nitride layer is formed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

3. A non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of said first silicon nitride layer is $10^{21}/cm^3$ or more.

4. A non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of said second silicon nitride layer is $10^{19}/cm^3$ or less.

5. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon nitride layer deposited on said silicon oxide layer and having a lower trap density than that of said silicon nitride layer formed by a CVD method.

6. A non-volatile semiconductor memory device according to claim 5, wherein said silicon oxide layer is deposited by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

7. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon oxide layer deposited on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

8. A non-volatile semiconductor memory device according to claim 7, wherein said silicon oxide layer is deposited by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

9. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a lower trap density than that of a silicon nitride layer formed by a CVD method.

10. A non-volatile semiconductor memory device according to claim 9, wherein said silicon nitride layer is formed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

11. A non-volatile semiconductor memory device according to claim 9, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said floating gate and said control gate, and

a silicon oxide layer is interposed in between said double-layered silicon nitride layers.

12. A non-volatile semiconductor memory device according to claim 9, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said floating gate and said control gate, and

a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between said double-layered silicon nitride layers.

13. A non-volatile semiconductor memory device

according to claim 9, wherein said silicon nitride layer is provided only on the side contiguous to said floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silicon oxide layer which are formed by the CVD method, are provided on said silicon nitride layer.

14. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

15. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layer is formed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

16. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said floating gate and said control gate, and

a silicon oxide layer is interposed in between said double-layered silicon nitride layers.

17. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said

floating gate and said control gate, and

a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between said double-layered silicon nitride layers.

18. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layer is provided only on the side contiguous to said floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silicon oxide layer which are formed by the CVD method, are provided on said silicon nitride layer.

ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory device according to the present invention has a semiconductor substrate and a memory cell having a floating gate provided through a tunnel insulating layer on the semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate. The inter-insulating layer includes a silicon oxide layer contiguous to said floating gate, a first silicon nitride layer provided by a CVD method on the silicon oxide layer and a second silicon nitride layer provided on said first silicon nitride layer and having a lower trap density than that of the first silicon nitride layer. The inter-insulating layer may includes a silicon oxide layer contiguous to said floating gate and a silicon oxide layer deposited on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less. The inter-insulating layer also may includes a silicon oxide layer serving as a layer contiguous to at least one of the floating gate and the control gate, and having a lower trap density than that of a silicon nitride layer formed by a CVD method.

FIG. 1A

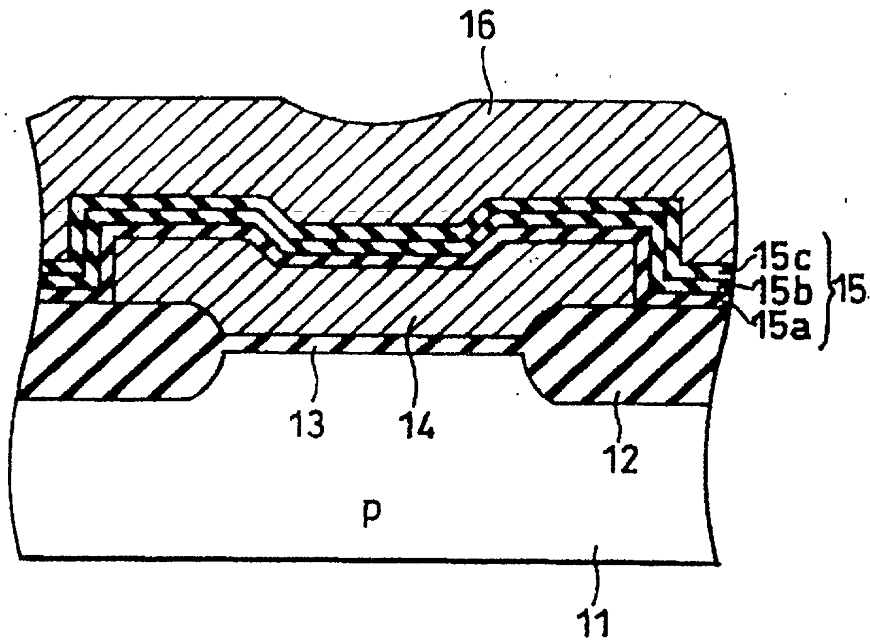
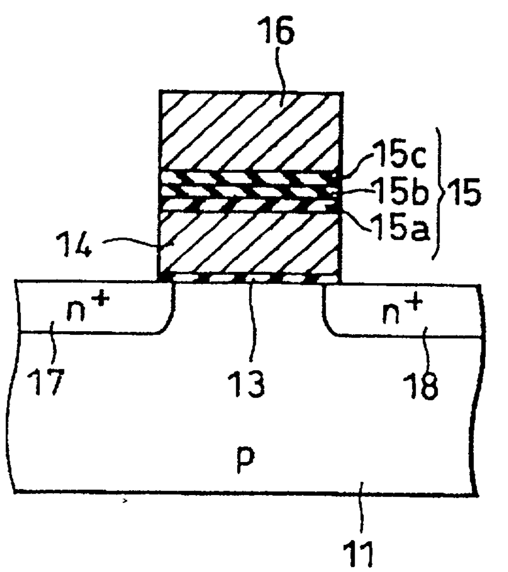


FIG. 1B



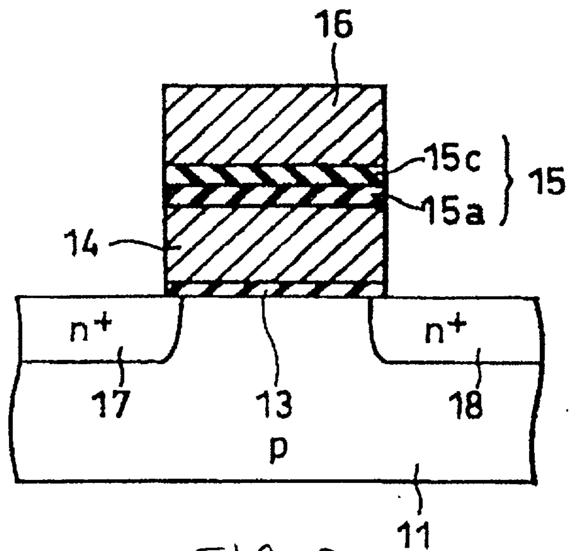


FIG. 2

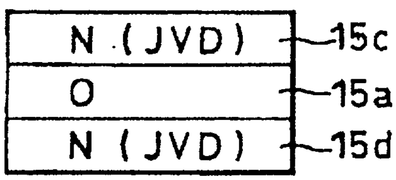


FIG. 3A

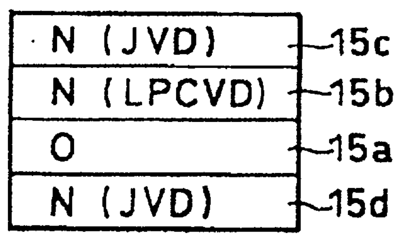


FIG. 3B

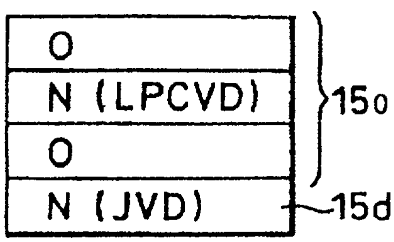


FIG. 3C

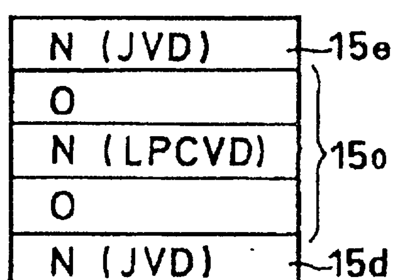


FIG. 3D

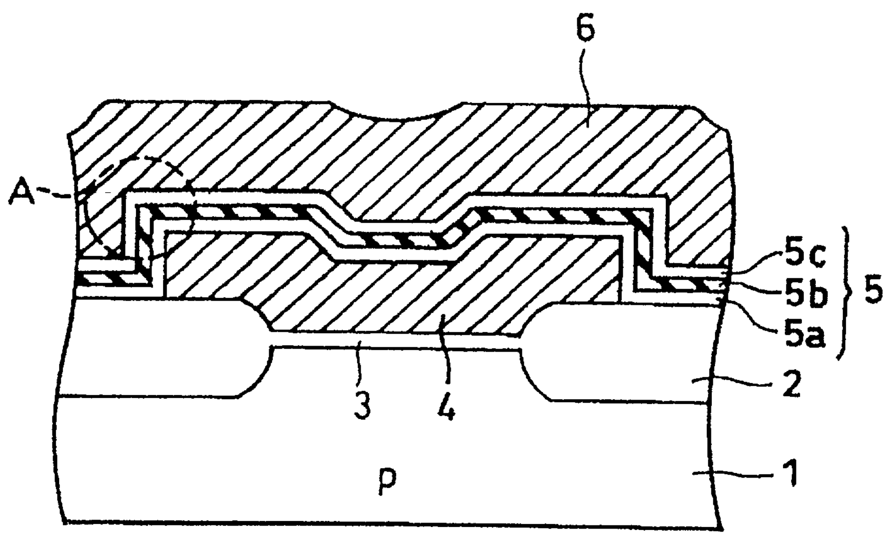


FIG. 4A

PRIOR ART

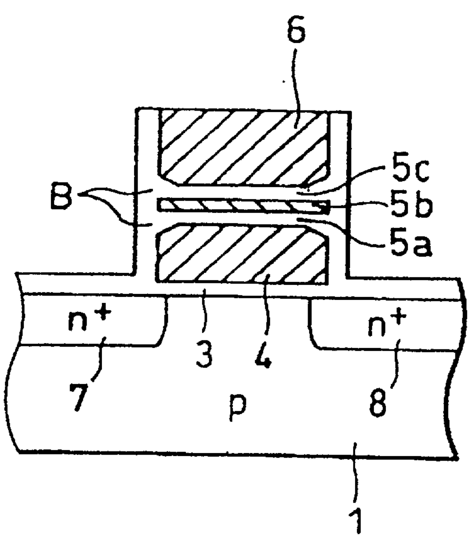


FIG. 4B

PRIOR ART

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

______

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ______に提出され、米国出願番号または
特許協定条約 国際出願番号を ______ とし、
（該当する場合） ______ に訂正されました。

☐ was filed on
as United States Application Number or
PCT International Application Number
and was amended on
______________________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条（ａ）－（ｄ)項又は３６５条(ｂ)項に基き下記の、米国以外の国の少なくとも１ヶ国を指定している特許協力条約３６５条(ａ)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
350232/1998	Japan	9/December/1998	☐
			☐

私は、第３５編米国法典１１９条(ｅ)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(ｃ)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/106 (8-96)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
（日本語宣言書）

委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと） Stuart Lubitz, (Reg. 20,680)William Wright (Reg. 36,312)Louis A. Mok (Reg. 22,585)Michael Ram (Reg. 26,379) John P. Scherlacher (Reg. 23,009)Hideo Koda (Reg. 27,729) Gary D. Mann (Reg. 34,867)Don F. Livornese (Reg. 32,040)	POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)* R. Dabney Eastham (Reg. 31,247)David L. Lubitz (Reg. 38,229) Jeffrey M. Hersh (Reg. 35,541)Peter Gluck (Reg. 38,022) Jonathan Kang (Reg. 38,199) Wei-ning Yang (Reg. 38,690)Mr. Alfred D'Andrea (Reg. 27,752)
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唯一または第一発明者名	Full name of sole or first inventor Seiichi MORI
発明者の署名 日付	Inventor's signature Date Seiichi Mori Dec. 6, 1999
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国籍 日本	Citizenship Japan
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第二共同発明者	Full name of second joint inventor, if any
第二共同発明者の署名 日付	Second inventor's signature Date
住所 日本国, ______	Residence , Japan
国籍 日本	Citizenship Japan
私書箱	Post Office Address
（第三以降の共同発明者についても同様に記載し、署名をすること）	(Supply similar information and signature for third and subsequent joint inventors.)